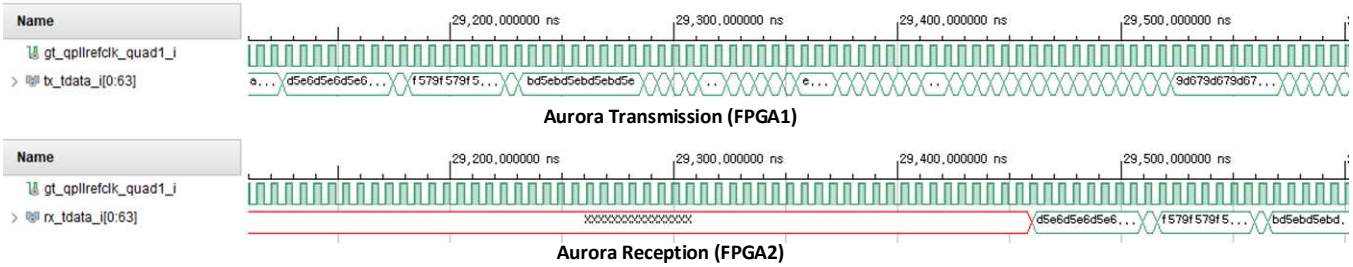

Figure 3. Operation of Aurora transmission and reception.

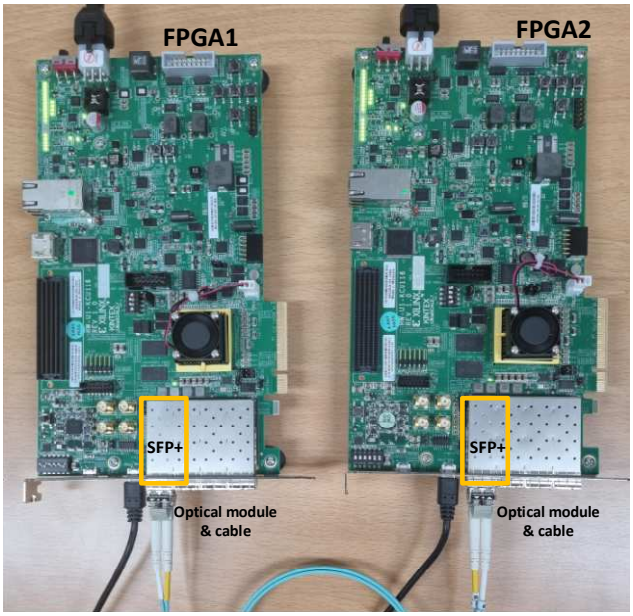

Figure 4. Connection of two evaluation boards.

Physical connection of Aurora lane can be implemented using SMA connector or SFP/SFP+ transceiver on the FPGA evaluation board. The SMA connector is connected with a 50Ω SMA cable, and the SFP/SFP+ transceiver is connected using optical modules and optical cables.

B. Data transmission and reception

In order to transmit and receive data through the aurora protocol, initializing process for the aurora channel is required. The initialization process consists of lane initialization and channel bonding. When all lanes are reset in the lane initialization process, it is ready to the channel bonding process. Channel bonding compensates the skew between lanes. When channel bonding is completed, in the case of simplex, it can freely transmit or receive data. In the case of duplex, it waits for the other party to prepare, then transmits or receives data.

Data received from the user application can be expressed in frames and blocks. A frame is a unit composed of 8 bits, and a block is composed of 8 frames. The data block is composed of frames through the link-layer frame delineation process, and the separator block is composed of bytes. Each data block is encoded including a sync header through a 64B/66B encoding process. The encoded data needs to be serialized. Since the data reception process reverses the transmission process, deserialization is performed. Then, the deserialized data block is received through a control block stripping process that classifies the type of control blocks and separates a sync header and a data block through 64B/66B decoding.

III. Experimental Results and Concolusions

Experiments are conducted using Xilinx FPGA to implement Aurora interface. Data transmission/reception between two KCU116 boards with built-in Kintex UltraScale+ chip is implemented. For circuit implementation, Vivado Design Suite 2021.2 is used, and Aurora hardware[3] is used. Aurora hardware is set to use one lane, lane rate is set to 10.3125 Gbps. The Giga-bit transceiver reference clock is set to 156.25MHz, and data flow mode was set to simplex. Figure 3 is configuration of hardware using two KCU 116 boards and SFP+ transceiver with optical modules and cable. Figure 4 shows the data transmitted and received through Aurora protocol in two FPGA evaluation boards. As shwon in Figure 4, when 64'hD5E6_ D5E6_D5E6_D5E6 is transmitted from TX of Aurora protocol implemented in FPGA 1, the data is received succesffuly from RX of FPGA 2.

In this paper, it was confirmed that complete data was transmitted and received by implementing the Aurora interface that supports communication between FPGAs. Therefore, by using the Aurora interface, it is possible to implement high-speed data transmission and reception using the Giga-bit transceiver of FPGA.

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